Electrical Simulations of Series and Parallel PV Arc-Faults

Jack Flicker and Jay Johnson
Sandia National Laboratories, Albuquerque, NM 87185, USA

***Abstract*—Arcing in PV systems has caused multiple residential and commercial rooftop fires. The *National Electrical Code*® (*NEC*) added section 690.11 to mitigate this danger by requiring arc-fault circuit interrupters (AFCI). Currently, the requirement is only for series arc-faults, but to fully protect PV installations from arc-fault-generated fires, parallel arc-faults must also be mitigated effectively. In order to de-energize a parallel arc-fault without module-level disconnects, the type of arc-fault must be identified so that proper action can be taken (e.g., opening the array for a series arc-fault and shorting for a parallel arc-fault). In this work, we investigate the electrical behavior of the PV system during series and parallel arc-faults to (a) understand the arcing power available from different faults, (b) identify electrical characteristics that differentiate the two fault types, and (c) determine the location of the fault based on current or voltage of the faulted array. This information can be used to improve arc-fault detector speed and functionality.**

***Index Terms*—SPICE, series and parallel arc faults, PV, AFD, AFCI**

I. INTRODUCTION

National Electrical Code® 690.11 only requires series arc-fault protection for PV systems [1]. This leaves the possibility of a parallel arc-fault establishing a fire. As a result, UL 1699B [2] provides a testing protocol for listing a Type 2 device capable of mitigating series and parallel arc-faults, and the PV industry is currently pursuing parallel arc-fault detection, differentiation, and mitigation techniques [3-5]. MidNite Solar, Inc. has developed the first series and parallel AFCI combiner box prototype, which first assumes a series arc-fault when there is arc-fault noise on the array and opens the string(s); then the AFCI rechecks for arcing noise and shorts the array to de-energize the parallel arc-fault if necessary. However, there are many alternative approaches to detecting and differentiating series and parallel arc-faults presented in previous work [3]; the simplest of which would be to monitor the high frequency noise created by the arc-fault in conjunction with the current and voltage of the array. Numerical and experimental studies were performed to determine the accuracy and robustness of using this method for a range of fault types, impedances, and locations.

Differentiating series and parallel arc-faults is important if the interrupting devices (IDs) of the Type 2 arc fault circuit interrupter (AFCI) are not located at each module. If the Type 2 AFCI is at the combiner or inverter, the arc-fault protection system must open the array if there is a series arc-fault and short the array if there is a parallel arc-fault. Unfortunately, if the wrong action is taken, the arc will continue and the fault power will increase.

To better understand the different fault types and determine if there is a surefire method of differentiating the faults, Sandia National Laboratories (SNL) has developed a PV array model [6] using a simulation program with integrated circuit emphasis (SPICE) [7]—a free node-based electrical modeling software—to better understand the electrical dynamics of the series and parallel arc-faults. The SPICE models of different arc-faults have been studied in hopes of creating a quick, accurate differentiation scheme between different types of parallel and series arc-faults using current/voltage information that is already being collected by the inverter during PV array operation.

In order to validate the SPICE model, a number of the simulated faults were compared to field experimental studies performed at the Distributed Energy Technologies Laboratory (DETL) at SNL using both a set of power resistors—which simulated solid ground faults, line-line faults, and increased series resistance in the PV string from damage or corrosion—and an arc-fault generator (AFG) similar to the one used in UL 1699B [4] to simulate:

1. series arc-faults in the string,
2. intra-string parallel arc-faults,
3. cross-string parallel arc-faults, and
4. arcing ground faults

To validate the inverter model and eliminate the transient dynamics of the inverter, a variable load bank surrogate was used and set to the maximum power point (MPP) of the unfaulted array. Therefore, all the fault types were conducted with all the combinations of load bank/inverter and resistor/AFG. The resistor situations with an inverter are shown in Figure 1. Note that the ground fault simulations were conducted by faulting to the grounded current carrying conductor as opposed to the equipment grounding conductor because the electrical behavior of the array is nearly the same and it would not clear the ground fault fuse.

Experiments and simulations were performed in parallel for the different test cases in the following order:

1. Resistance faults with the load bank were studied to find SPICE parameters for the PV modules and provide a baseline for the other tests.
2. Arc-faults with the load bank were studied to ensure the SPICE arc-fault model (a resistor) accurately simulated the dynamic electrical behavior of arc plasmas.
3. Numerical and experimental studies of solid ground faults, series faults, and line-line faults were used to analyze the behavior of faulted PV systems with an inverter.

4. Experimental tests and simulation-based verification of different arc-faults was used to determine the type and location of the fault.

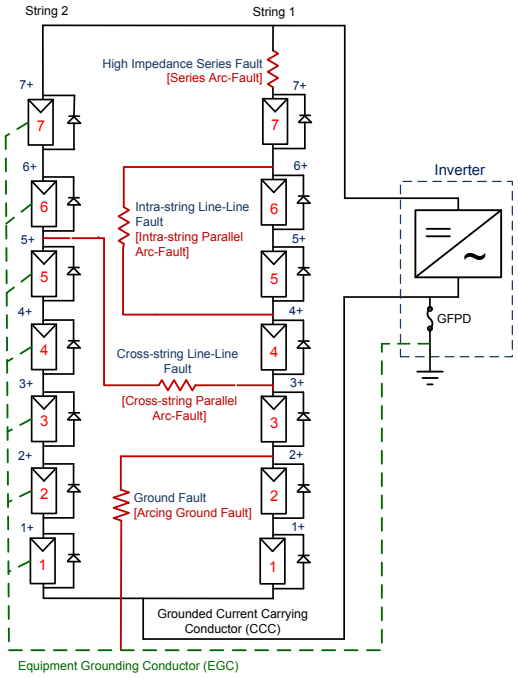


Fig. 1. Different types of series and parallel solid faults (blue) and arc-faults (red, bracketed) on the DC side of a PV array composed of two strings.

II. PV MODEL

Computer circuit simulations are able to model non-linear PV circuits for a wide variety of conditions [8]. A common method of circuit simulation is the use of SPICE. In this work, MacSPICE is used to analyze the behavior of a PV array during various arc-fault conditions [9, 10].

The SPICE model of the PV array uses a single module as the base building block. The construction of a single module is accomplished using a standard one-diode model [6]. This model consists of an ideal current source with a value equal to the module short-circuit current (I_{sc}) in parallel with a diode and shunt resistance (R_{sh}) all in series with a series resistance (R_s). In order to increase the V_{oc} of the module above the voltage drop of a regular diode (~0.6 V), the ideality constant of the diode (N) must be increased [9].

The one-diode model was constructed to approximate the IV curve of 200 W monocrystalline Si modules located at DETL. The parameters of the one-diode model change for each simulation to account for changes in solar irradiance and module operation temperature. For an irradiance of 900 W/m^2, the current source is set to supply 3.2 A at short circuit (SC), the diode has an ideality factor of N=131 and leakage current $I_o=2.85\cdot10^{-8}$ A, R_{sh} is set 550 Ω and the R_s is set to 900 mΩ. This module gives an IV curve with I_{sc} of 3.2 A, V_{oc} of 63.24 V, and P_{mp} of 137.5 W. The max power point (MPP) has I_{mp}=2.67 A and V_{mp}=51.5 V.

The PV array model is comprised of two strings wired in parallel. Each string is composed of seven modules in series. Each module is connected to a bypass diode ($I_o=4.7\cdot10^{-12}$ A, N=1). For the purposes of simulation, the fault location is denoted by "n+" notation, where n+ indicates the fault position at the positive terminal of the nth module above the grounded CCC.

In each simulation, the PV array is constructed with multiple modules connected to a central load that approximates the impedance of the inverter or load bank used in the experimental conditions. The arc-fault is modeled by a simple resistor with the resistance determined by the ratio of the measured median arc voltage to the median arc current for each fault scenario.

The results from the constant resistance fault with a load bank were used to generate the PV module parameters for the simulations. The model errors are shown in Fig. 2 for the different fault types. The fault errors are often larger than the array errors because of the small values and measurement error.

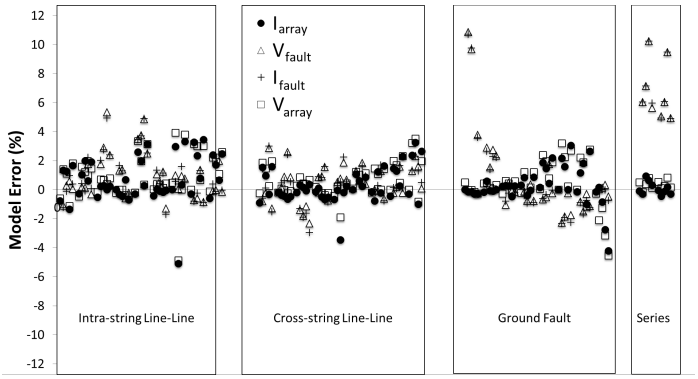


Fig. 2. Model errors for the resistor fault and load bank.

III. THEORETICAL DIFFERENTIATION OF ARC-FAULT TYPES AND FAULT FINDING

The primary goals of the simulations are to (a) determine the type of arc-fault (series vs. parallel) using measurements at the inverter (array current and voltage) so that proper de-energization procedures (opening or shorting) can be performed and to determine where arc-faults occurred using the IV curve of the array. Note that after a series arc-fault has been mitigated, the burned/damaged conductor will likely be open and easily located, but after a parallel arc-fault, there may be no change in the array IV curve because there is no longer a conduction path between the parallel conductors. Therefore, determining the location of the parallel arc-fault would have to be performed while the arc existed. However, these techniques could be used to locate line-line faults.

A. Series arc-faults

Ideal PV arrays have near zero impedance in module interconnects and connectors. Series faults occur due to degradation in solder joins, PV wiring, or junction boxes, increasing the interconnect impedance above its nominal

value. These faults and series arc-faults act much like an increase in R_s in a specific module [11]. For a small increase in impedance, both array I_{sc} and V_{oc} are unchanged, while the fill factor of the array IV curve decreases (Fig. 3). As the interconnect impedance increases above ~60 Ω, the array I_{sc} monotonically decreases while the array V_{oc} remains unchanged. Experimental series arc-faults had resistance values between 5-25 Ω, however, so there were only slight changes to the IV curve of the array.

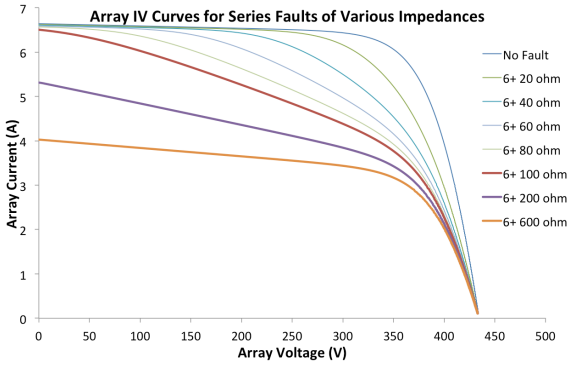


Fig. 3. Effect of series fault of different impedances on array IV curve

For series arc-faults, the IV curve of the array is independent of the location of the series fault so this method cannot be used to determine the fault location (Fig. 4), but an IV curve could be used to estimate fault impedance using I_{sc} or fill factor (FF) as an indicator (Fig. 5).

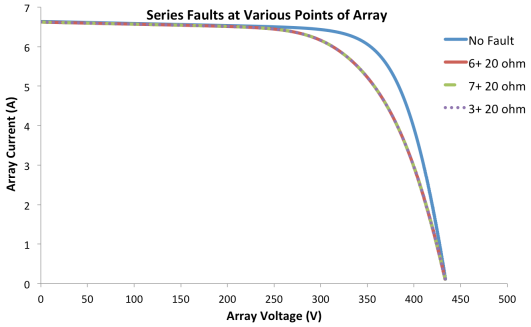


Fig. 4. Series faults at different locations of the array cause identical effects on the array IV curve and, therefore, cannot be resolved

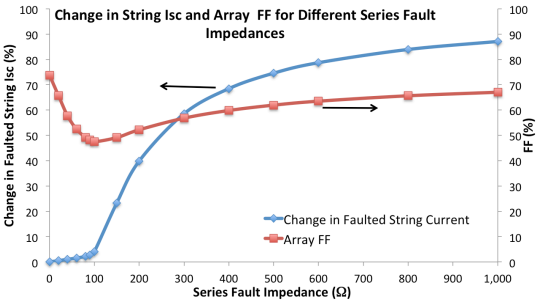


Fig. 5. Series fault impedance affects both array FF and the I_{sc} of the shorted string. These parameters can be used to estimate the fault impedance

B. Parallel arc-faults

Parallel arc-faults come in three varieties: cross-string, intra-string, and ground. These faults are especially dangerous since (unlike series arc-faults) a pathway exists for fault current to flow even when the array is open, posing both a fire and shock hazard. In each type of parallel arc-fault/line-line, the symmetry of the array is altered and the faulted string appears to be composed of fewer modules than in the unfaulted case. This has the effect of decreasing the V_{oc} proportional to the number of modules while leaving I_{sc} unaffected, shown in Fig. 6.

Parallel arc-faults that bypass different numbers of modules are relatively easy to differentiate from each other due to the large changes in V_{mp} and V_{oc}. The differentiation between fault types that bypass the same number of modules is slightly more complex. It is not possible to resolve the location of intra-string parallel arc-faults or arcing ground faults from either the array current or voltage. This is because the IV curve of a faulted string is identical regardless of which module is faulted (Fig. 7) and is dependent only on the fault impedance and number of modules bypassed.

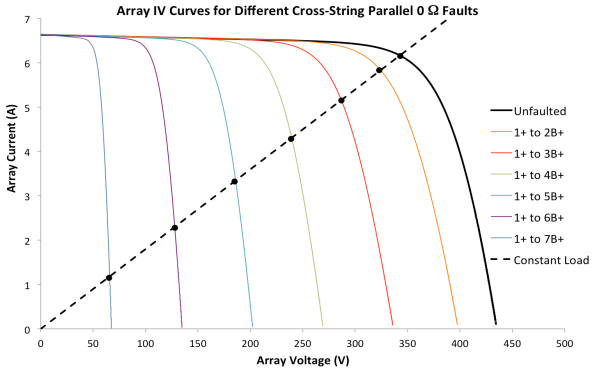


Fig. 6. Cross-string parallel faults (2nd string module location designated with the 'B') decrease array V_{mp} and V_{oc}. This decrease is a linear function of the number of modules bypassed by the fault and the same for intra-string arc-faults and arcing ground faults.

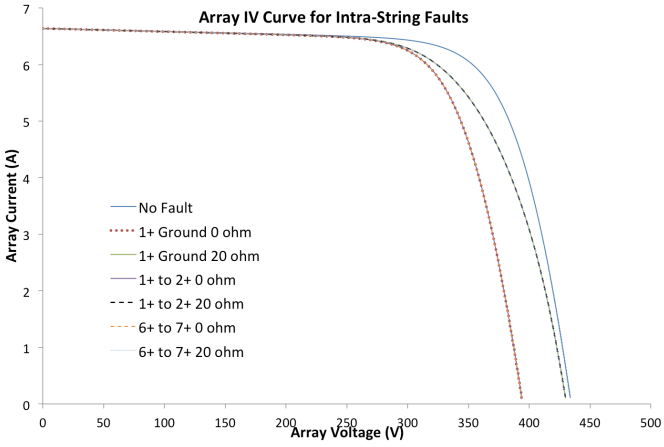


Fig. 7. Intra-string faults impact the array IV curve similarly, making it impossible to discern their location from array electrical measurements. This behavior exists for ground faults and intra-string line-line faults as well [10].

Unlike intra-string faults, the location of cross-string faults is identifiable if precision measurements of the IV curve are possible. The V_{oc} of a PV array under a cross-string fault does depend slightly on the position of the fault (Fig. 8) due to module non-idealities in the current pathway (most likely added values of R_{sh}). Unlike the intra-string fault, where the unfaulted string IV curve is identical before and after the fault, in a cross-string fault, both strings are effected; and due to the presence of series resistance in the modules, this changes the V_{oc} for the two strings and yields a slight mismatch dependent on fault position.

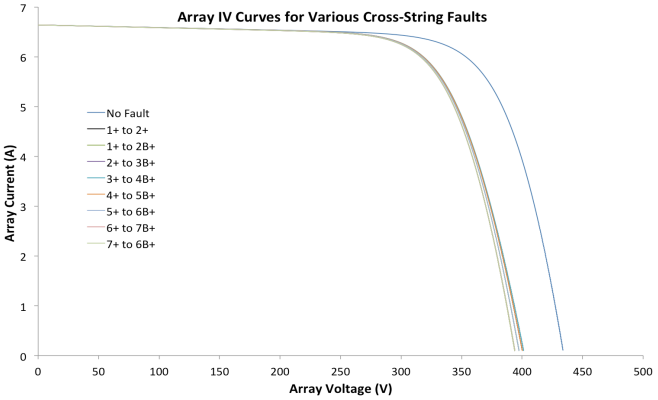


Fig. 8. Cross-string faults impact the array V_{oc} differently depending on fault location in the array. The position of the cross-string fault can, theoretically, be determined through electrical measurements.

C. Differentiation of Series, Intra-, and Cross-string Faults

The range of fault types, locations, and impedances, make it difficult to differentiate between series and parallel arc-faults based purely on array IV behavior. Depending on the exact meteorological conditions, each fault could have nearly the same effects on the array IV curve, especially at MPP (Fig. 9). Therefore, based on the steady-state SPICE model, differentiation between series and parallel faults cannot be achieved through current and voltage measurement at the inverter.

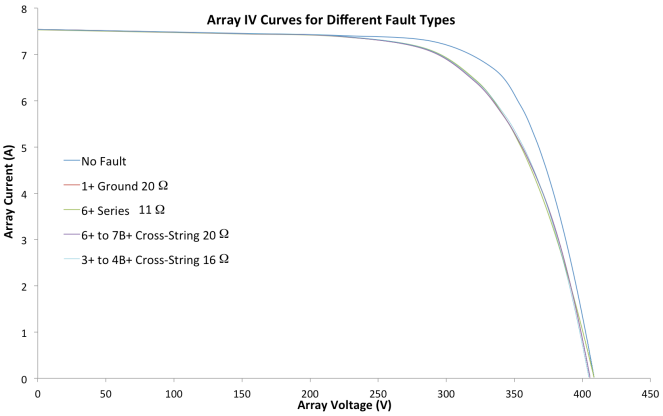


Fig. 9. Without knowing either the type of fault or fault impedance, it may be difficult to determine both from electrical measurements since they have similar effects on the array IV curve.

IV. EXPERIMENTAL ARC-FAULT TESTS AND MODEL VALIDATION

In order to validate the SPICE model and expand on the work in [6], a series of arc-fault tests were performed on real PV arrays at DETL composed of two parallel strings of seven 200 W monocrystalline Si modules connected in series. In each experiment, the fault was installed between modules using MC4 T-branch connectors. The fault and array current and voltage were collected with a Tektronix DPO3014 oscilloscope, two Tektronix P5200 differential voltage probes, and two Tektronix TCP303 current probes.

A. Constant resistance fault with load bank

The PV array was connected to a load bank with impedance (55.6 Ω) approximately equal to the array MPP and resistive faults of 3.2, 5.1, 10.5, and 22.4 Ω were established for each of the fault types. To calibrate the SPICE model to the unfaulted array and to validate the model for the faulted array, IV curves were taken of the array using a Daystar, Inc DS-100C IV curve tracer. The model closely predicted the IV curve for intra-string faults, such as the 2+ to 1+ example shown in Fig. 10.

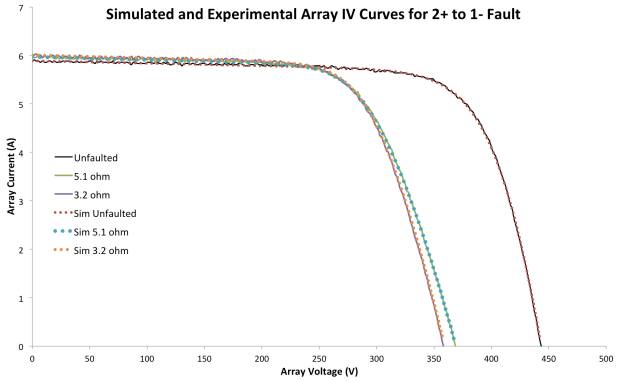


Fig. 10. Experimental IV curves of faulted and unfaulted states (solid lines) overlaid with SPICE simulations (dots).

Fig. 11 shows the results of array current and voltage for the four different faults with the 5.1 Ω resistor and load bank. The array current and voltage shows a linear dependence on number of modules faulted, nearly independent of fault type (differences are most likely due to changing environmental conditions such as irradiance and temperature), as predicted by theory (Fig. 6). The solid line denotes the load bank line (55.6 Ω). The fault impedance controls the spacing of points along the line. High impedance faults lie close together at high voltage and current values since those faults yield smaller drops in faulted array voltage and current. Low impedance faults are spread farther out along the load line.

Fig. 12 shows the results of experimental ground fault tests of the PV array using the resistors. The top figure shows fault current/voltage information. The dashed lines indicate the different resistances used for the faults. The bottom figure shows excellent correlation between array current/voltage

information for the experiments and SPICE simulations. The dashed line shows the load bank impedance (55.6 Ω).

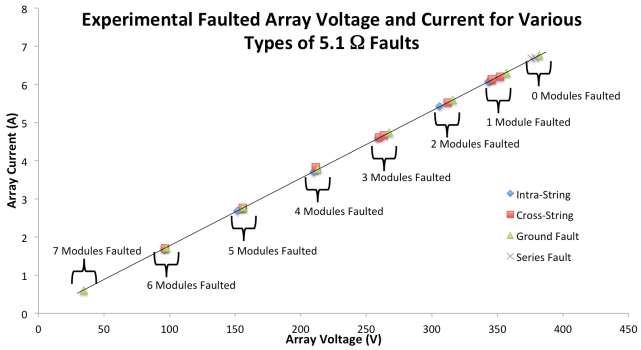
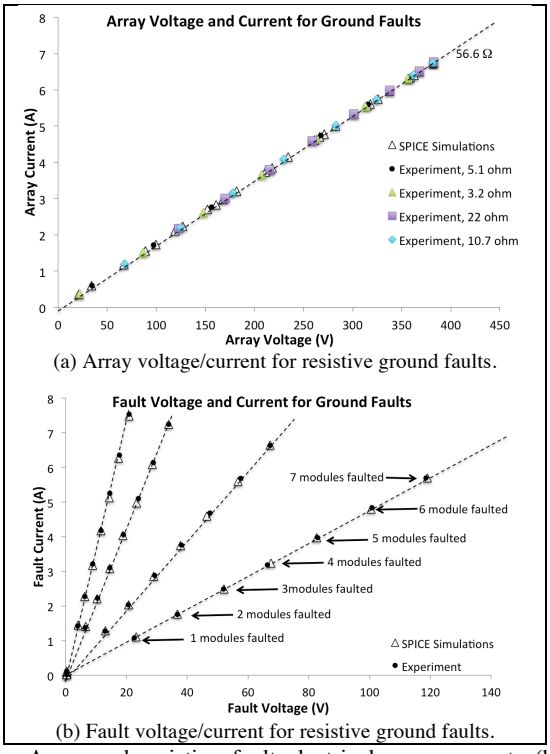


Fig. 11. Results of faulted array current and voltage for various types of faults for a fault impedance of 5.1 Ω.



(a) Array voltage/current for resistive ground faults.

(b) Fault voltage/current for resistive ground faults.

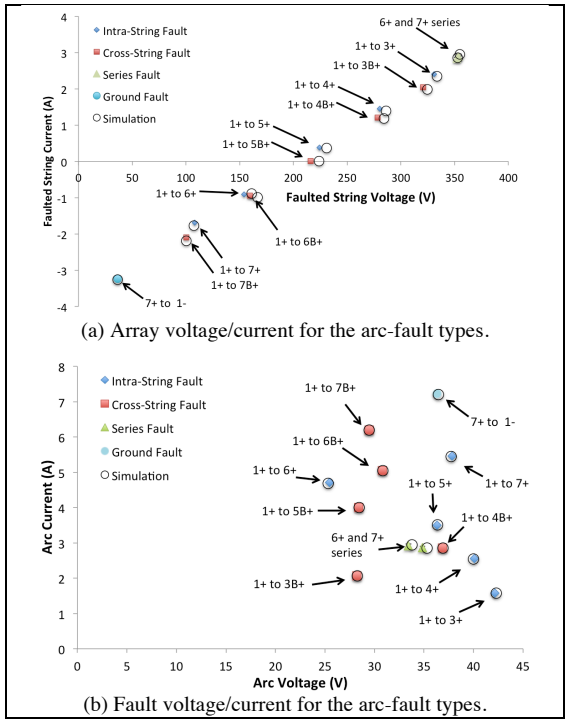
Fig. 12. Array and resistive fault electrical measurements (black) and SPICE simulations (white) for ground faults.

The SPICE simulations match the experimental data points well (<5% error) for all fault conditions studied. Similar matching results were obtained for cross-string, series, and intra-string faults. As more modules are faulted, the SPICE simulations slightly underpredict both the fault current and fault voltage. This error can be due to differences in the fault resistance between simulation and experiment, a slight mismatch in the series resistance of the module model, or parasitic resistances due to PV wiring and interconnects.

B.Arc-fault tests with load bank

Having demonstrated that the SPICE simulations accurately predict well-behaved and well-characterized constant resistance faults, arc-fault experimental data was compared to the simulations. As opposed to a constant resistance, arc faults have a time-variable, current-dependent resistance. The arc-faults were generated using the procedure highlighted in [12]. For the purposes of simulation, the arc resistance was calculated using the ratio of the measured arc voltage and current.

The results of the experimental tests and corresponding SPICE simulations are shown in Fig. 13 for ground faults, series faults, cross-string faults, and intra-string faults. The SPICE simulations match well with the experimentally collected data points (<5% error), though the simulations overestimate the faulted string voltage. It is interesting to note the back-fed current through the faulted string during array operation for faults that incorporate five or more modules.



(a) Array voltage/current for the arc-fault types.

(b) Fault voltage/current for the arc-fault types.

Fig. 13. Experimental (colored points) and SPICE simulations (white circles) of the four different arc-faults with a load bank.

C. Arc-fault tests with inverter

In order to test if the SPICE simulations could accurately predict inverter operation under arc-fault conditions, the array was connected to a 5.0 kW inverter without arc-fault protection. Series arc-faults have been previously analyzed [12] and are omitted here for brevity. It was found during testing that the inverter responded similarly for both constant resistance faults and arc-faults. Furthermore, for both constant resistance faults and arc-faults, the inverter responded to parallel, ground, or line-line faults in three different ways depending on fault "severity," i.e. the number of modules faulted and the fault impedance (Fig. 14). Fig. 15 shows the measured array voltage traces and corresponding matching SPICE simulations during the three operating conditions.

For high impedance faults or a small number of modules faulted (blue trace in Fig. 15), the inverter continued to operate through the fault as expected by the SPICE simulations. When a fault occurs, the new array operating point (OP) jumps along a constant load line to the faulted IV curve. However, ~40 ms after the fault, during the bus capacitor discharge, the inverter senses the change of state and increases the load impedance to operate at the same voltage as $MPP_{unfaulted}$. The inverter will then maximum power point track (MPPT) and decrease the load impedance to reach $MPP_{faulted}$ (the time scale in Fig. 15 is too short to show MPPT during the fault). Once the fault is cleared, the OP instantly changes along a constant load line to the unfaulted IV curve. Then, again after ~40 ms, the array changes its impedance to operate at the same voltage as $MPP_{unfaulted}$. This mode of operation is beneficial for arc-fault suppression since the tracking of the inverter during the fault (decreasing load impedance to reach $MPP_{faulted}$) decreases current through the fault and may extinguishing the arc-fault.

For slightly lower impedance faults or when more modules are bypassed (red trace in Fig. 15), the inverter pauses MPPT. In this mode, the inverter does not MPPT through the fault, but instead goes to $V_{oc\text{-}faulted}$ and stays there throughout the duration of the fault. Once the fault is cleared, the inverter OP becomes $V_{oc\text{-}unfaulted}$ and the inverter moves the OP to $MPP_{unfaulted}$. This operation mode is not ideal for parallel faults since, at OC, the entire array power is diverted through the fault pathway, posing a serious fire hazard.

Finally, for a low impedance fault across a large number of modules (green trace in Fig. 16), the presence of the fault will cause the inverter to die. In this mode, the inverter momentary holds the array voltage at ~220 V (minimum input voltage is 250 V), during which a large negative current flows through the array, indicating back streaming from the AC-side of the inverter. The period that the array is held at this voltage is proportional to the "severity" of the fault. For example, during a 7+ to 1- line-to-line fault, the array will only be held at this voltage for a few milliseconds, as opposed to a 4+ to 1- fault, where the voltage is held for nearly one second. After the array is held at ~220 V for a period of time, the array voltage collapses to $V_{oc\text{-}faulted}$ and remains there until the fault is cleared. Once the fault is cleared, the OP changes to $V_{oc\text{-}unfaulted}$ and stays there as the inverter restarts (typically, five minutes).

This operation mode is extremely dangerous in the presence of parallel arc-faults. By holding the voltage constant and allowing back fed current to flow to the array from the AC-side, the inverter is increasing power through the fault pathway above the maximum power of the array. Then, when the voltage collapses to $V_{oc\text{-}faulted}$, all the array current flows through the fault pathway for the duration of the fault.

Due to the dependence of the inverter operating state on fault resistance and number of modules faulted, the trigger for these operating modes is most likely input voltage to the inverter.

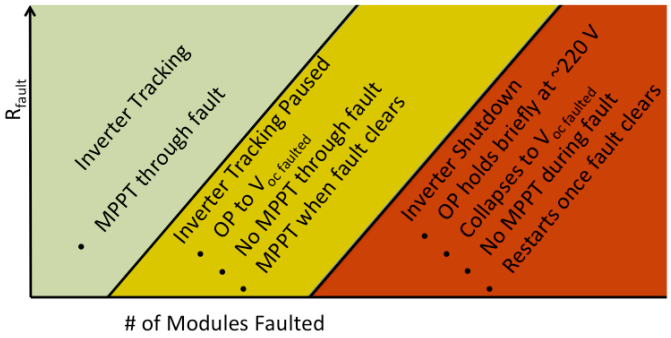


Fig. 14. Three different modes of inverter operation were found depending on the "severity" of the fault.

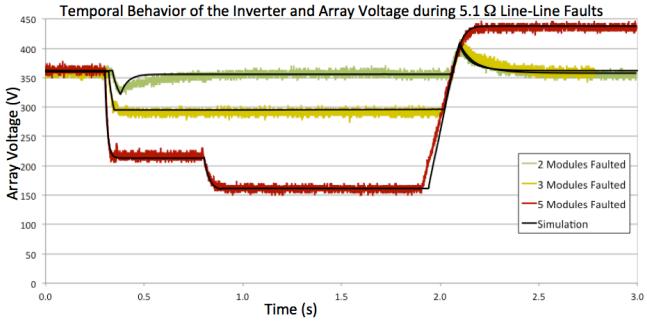


Fig. 15. Array voltage over time for three different inverter operating modes showing both measured data (colored traces) and corresponding SPICE simulations (black traces)

In order to match the SPICE simulation to inverter operation, a 5.1 Ω, 2+ to 1- fault was created (this fault is in the "Tracking" operating regime of the inverter) and the inverter was allowed to undergo MPPT. Fig. 16 shows the measured data before, during, and after the fault. The corresponding SPICE simulations are denoted by black lines. The inverter impedance was measured during inverter operation (Fig. 17) and used for the SPICE simulations.

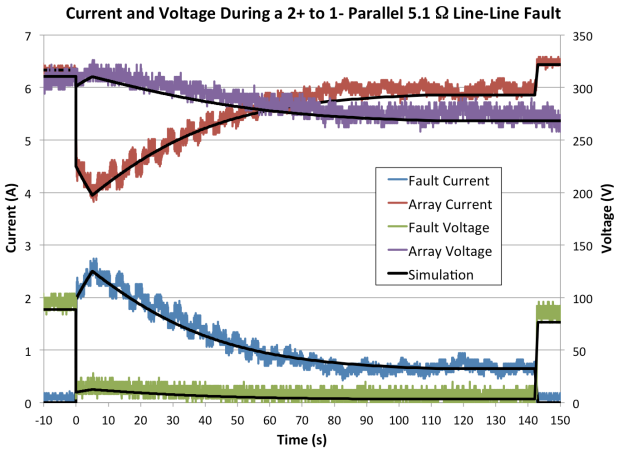


Fig. 16. Array and fault current vs. time for an arc fault connected to an inverter. The black lines show expected fault and array currents.

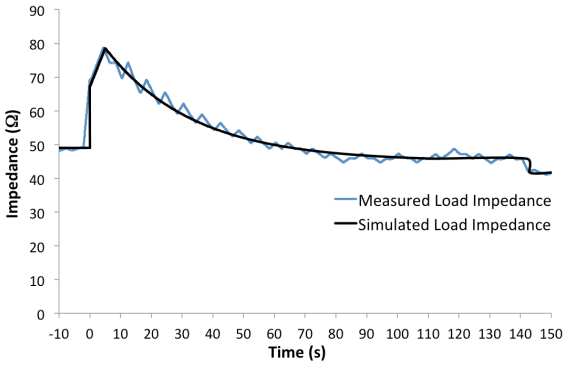


Fig. 17. Inverter impedance during the 5.1 Ω, 2+ to 1- fault.

Before the fault, the inverter impedance is 49 Ω, which corresponds to $R_{mp\text{-}unfaulted}$. When the fault occurs, the inverter "immediately" changes its impedance to 67 Ω in order to hold the array voltage constant (the change is not immediate; however the time step in the experiment is too large to see the voltage transient, as in the blue trace of Fig. 15). After the fault initiation, the inverter impedance tracks slightly in the incorrect direction (it increases linearly from 67 Ω to 78.6 Ω for 4.4 seconds) before the MPPT algorithm begins to decrease the inverter impedance towards $MPP_{faulted}$ ($R_{mp\text{-}faulted}$=45.83 Ω). The R_{load} determined by the MPPT algorithm was modeled in SPICE with Eq. (1).

$$R_{load} = 33.6 \cdot e^{-0.035t} + 45 \quad (1)$$

The MPPT algorithm holds the value of R_{load} relatively steady at $R_{mp\text{-}faulted}$ until the fault is cleared at 143 seconds. The inverter then "immediately" decreases its impedance to 41.7 Ω in order to keep the array voltage constant. As can be seen from Fig. 16, the SPICE simulations match all the measured values well and can completely describe both array and inverter behavior before, during, and after the fault.

Similar inverter behavior is seen with parallel arc-faults with the inverter. The inverter can continue MPPT, pause MPPT, or fall below the input voltage and shut down. As shown in Fig. 18, the array and fault electrical behavior is similar to the resistive fault, except that there is a high frequency noise added to the current and voltage measurements (consistent with arc-faults [12]). This additional noise appears to confuse the MPPT algorithm slightly, but the inverter still tracks up the IV curve toward $MPP_{faulted}$. In this test the arc-fault was sustained for as long as possible but because the MPP tracking decreases the inverter impedance, more fault current passes through the inverter, and less through the parallel arc-fault, until eventually it self-extinguishes.

These results show the difficulty in modeling arc-faults on real PV systems. While simplifying the arc-fault to a resistance element matches well, the inverter logic and operating characteristics (minimum input voltage, MPPT algorithm, AC backfeed, etc.) make it challenging to match experimental results with SPICE simulations that assume the inverter acts as a constant resistance load.

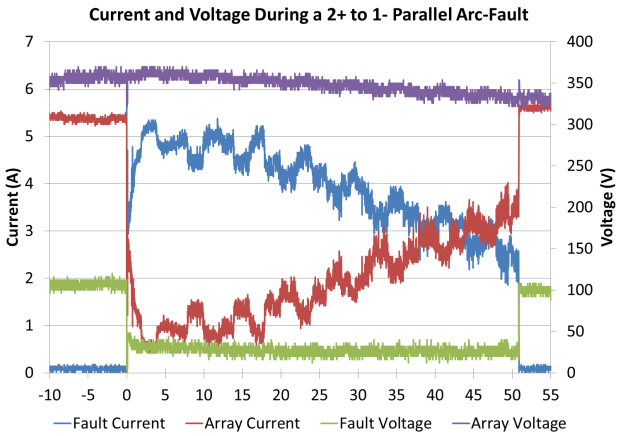


Fig. 18. Intra-string arc-fault array and fault current and voltage behavior when the inverter continues to MPP track.

V. SUMMARY AND CONCLUSIONS

This paper has introduced a method of modeling series and parallel arc-faults in PV arrays using SPICE simulations. Using this model and a range of experimental tests, the effects of series and parallel arc-faults and solid faults (e.g., line-line, high impedance series) on array electrical characteristics were determined.

In order to validate that SPICE model, experiments were carried out on real PV arrays at the DETL facility at Sandia National Laboratories. Four sets of experiments were carried out: constant fault resistance with load bank, arc fault with load bank, constant fault resistance with inverter, and arc fault with inverter. SPICE correctly predicted (error <11%) for the fault current/voltage and faulted array current/voltage for both the load bank cases. It was found that modeling the arc-fault as a time-varying resistance was successful, but modeling the inverter as a resistor at MPPT did not capture the sophisticated inverter controls.

While inverter operation was similar for both constant resistance faults and arc-faults, it was found that the inverter responded to faults in three different modes depending on fault "severity". For high impedance faults that encompassed only a few modules, the inverter would MPP track during the fault. For lower impedance faults that encompassed more modules, the inverter operated at $V_{oc\text{-}faulted}$ until the fault was cleared, after which the inverter operated normally. Finally, for very severe faults, the inverter attempted to hold the array at ~220 V, back feeding current from the AC-side before the array voltage eventually collapsed to $V_{oc\text{-}faulted}$. After the fault was cleared, the inverter stayed at $V_{oc\text{-}unfaulted}$ while it restarted.

SPICE simulations were able to completely describe all the inverter modes. SPICE was also able to accurately simulate the inverter behavior before, during, and after a 2+ to 1-, 5.1 Ω fault, including inverter MPPT algorithm behavior.

The simulations and experiments showed that certain types of faults are more powerful, and therefore more dangerous. The fault current and voltage varied linearly with number of modules faulted and the resistance of the fault. Therefore, faulting a larger number of models produces higher-power

arcs. The arc-faults across more modules are also more dangerous and difficult to extinguish because the inverter stops MPPT or shuts down entirely.

It was discovered that the fault type can be determined in some situations for solidly bonded faults if the IV curve can be taken of individual strings. Parallel faults can be identified by a change in the array V_{oc}. However, differentiating between the different parallel faults (intra-string, cross-string, and ground) is very difficult. Unfortunately, IV curve measurements are not possible during series and parallel arc-faults since series arc-faults will be extinguished at V_{oc} and parallel arc-faults will be extinguished at I_{sc}.

Table 1 summarizes the ability of electrical behavior to detect the location of the fault. Series, intra-string, and ground faults yield the same string and array IV curves regardless of fault location, so it is not possible to resolve their location from electrical measurements. However, it may be possible to determine which string is faulted by monitoring individual string currents. Array V_{oc} has a slight dependence on the location of cross-string faults, making it theoretically possible to determine their position purely from array electrical measurements.

Table 1. Summary of results from SPICE simulations showing if the location of faults can be determined from electrical measurements.

	Determine Fault Location?			
Type	**Array V_{oc}**	**Array I_{sc}**	**String I @ SC**	**String I @ OC**
Series	No	No	No	No
Intra-string	No	No	No	No
Cross-string	Yes	No	No	Yes
Arcing Ground	No	No	No	No

ACKNOWLEDGEMENTS

This work was funded by the DOE Office of Energy Efficiency and Renewable Energy. Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

REFERENCES

[1] National Electric Code, "NFPA 70," National Fire Protection Association. Quincy, MA, 2011.

[2] Underwriters Laboratories, "Photovoltaic (PV) DC Arc-Fault Circuit Protection," UL1699B, 2011.

[3] J. Johnson, M. Montoya, S. McCalmont, G. Katzir, F. Fuks, J. Earle, A. Fresquez, S. Gonzalez, and J. Granata, "Differentiating Series and Parallel Photovoltaic Arc-Faults," *38th Photovoltaic Specialists Conference (PVSC),* 2012.

[4] H. Haeberlin, "Arc detector as an external accessory device for PV inverters for remote detection of dangerous arcs on the DC side of PV plants," *Photovoltaic Solar Energy Conference Valencia,* 2010.

[5] J. Johnson, B. Gudgel, A. Meares, and A. Fresquez, "Series and Parallel Arc-Fault Circuit Interrupter Tests," *Sandia National Laboratories Technical Report, In Press,* May 2013.

[6] J. Flicker and J. Johnson, "Photovoltaic Ground Fault and Blind Spot Electrical Simulations " Sandia National Laboratories, 2013. Available: http://energy.sandia.gov/wp/wp-content/gallery/uploads/SAND2013-3459-Photovoltaic-Ground-Fault-and-Blind-Spot-Electrical-Simulations.pdf

[7] L. W. Nagel and D. O. Pederson, "SPICE (Simulation Program with Integrated Circuit Emphasis)." vol. ERL-M382, ed: University of California, Berkeley, 1973, p. 62.

[8] A. Devasia and S. K. Kurinec, "Teaching solar cell I-V characteristics using SPICE," *American Journal of Physics,* vol. 79 (12), p. 1232, 2011.

[9] L. Castaner and S. Silvestre, *Modelling Photovoltaic Systems using PSPICE*. Chichester, West Sussex, England: John Wiley and Sons Ltd, 2002.

[10] Y. Zhao, J. de Palma, J. Mosesian, R. Lyons, and B. Lehman, "Line-Line Fault Analysis and Protection Challenges in Solar Photovoltaic Arrays," 2009.

[11] E. E. van Dyk and E. L. Meyer, "Analysis of the effect of parasitic resistances on the performance of photovoltaic modules," *Renewable Energy,* vol. 29 (3), pp. 333-344, Apr 2004.

[12] J. Johnson, B. Pahl, C. Luebke, T. Pier, T. Miller, J. Strauch, S. Kuszmaul, and W. P. S. C. P. t. I. Bower, "Photovoltaic DC Arc Fault Detector testing at Sandia National Laboratories," Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE.